Variation Components and specific impact on SRAM

Ref1 Ohbayashi2007

Motivation

- How to overcome SRAM functionality challenges associated with process and cell design related variability

Claims

- Need R and W assist due to variability at 65nm
- SRAM bit cell layout a factor for variability
- Propose improved variation cell layout
- Single power supply optimal for SoC SRAM designs
- Process corner-compensating WLdroop Read assist
- Capacitive cell Vdroop for "fast and easy" Write assist
- Improved R&W margin with assist techniques and new cell layout

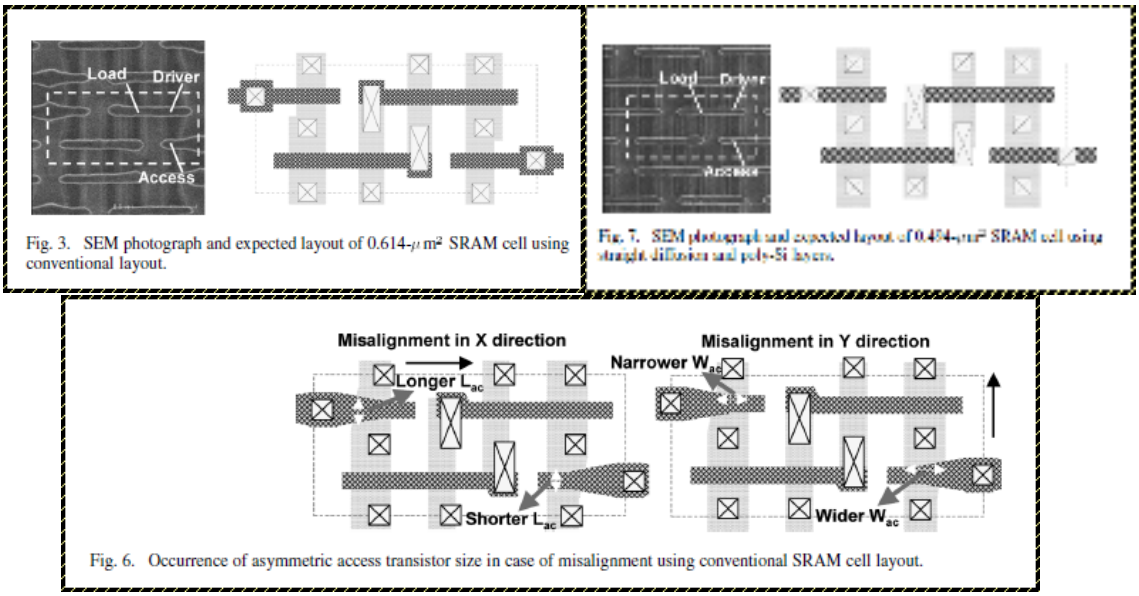

Fig. 3. SEM photograph and expected layout of 0.614-μ m² SRAM cell using conventional layout.

Fig. 7. SEM photograph and expected layout of 0.484-μm² SRAM cell using straight diffusion and poly-Si layers.

Fig. 6. Occurrence of asymmetric access transistor size in case of misalignment using conventional SRAM cell layout.

Other sources of variation in SRAM cell include:
-sti stress, well proximity, halo shadowing, corner rounding, line foreshortening,
-Well alignment, n+ or p+ poly doping encroachment

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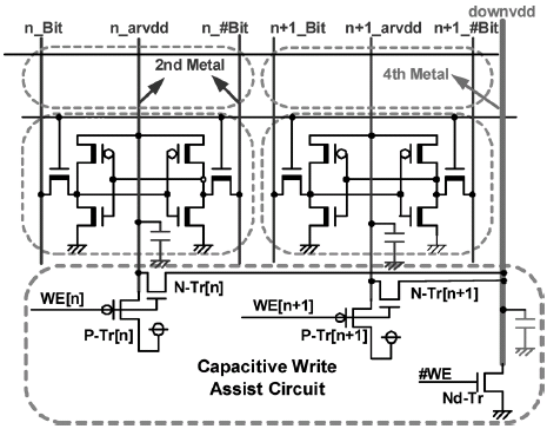
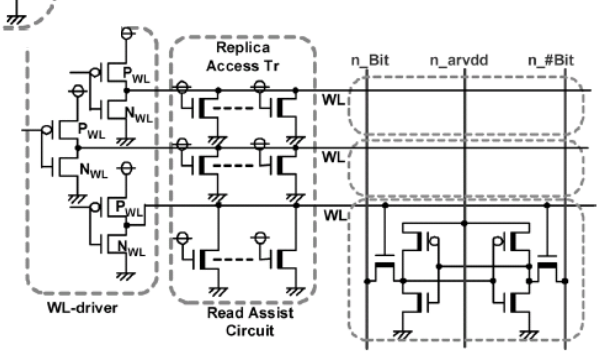


After that, the voltage level of the n_arvdd line falls in proportion to the capacity ratio between the arvdd and downvdd lines. Because of the falling voltage of the arvdd line in the selected column, the weaker pMOS drivability of the memory cell allows easier write operations. Because the write assist circuit utilizes the wiring capacitance of the downvdd line, the area penalty of this scheme is small.

the SNM of the straight cell in the high Vdd region is improved by the presence of the read assist circuit, because the electric ratio is improved.



The amount of WL droop will vary as the process varies. Chips with strong PGs will droopWL more.

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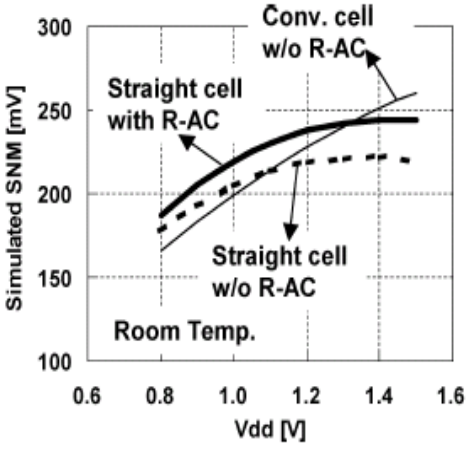
Major Results

Each WL is connected to several normally-on replica access transistors (RATs). A RAT has the almost same topological layout structure as the SRAM access transistor. The number of RATs required to be connected to a WL is less than 20. Therefore, the RATs' active current is negligible with a large SRAM macro having many columns such as 128, 256, or 512. In general, if the SRAM VthN is low, the SNM is small, and if the SRAM VthN is high, the SNM is large. The selected WL level is determined by the on-resistance ratio of the to RATs. If the SRAM VthN is lower, the access transistor's current is suppressed due to the lower WL level. Therefore, the electric ratio (see Fig. 5) and the SNM are maintained



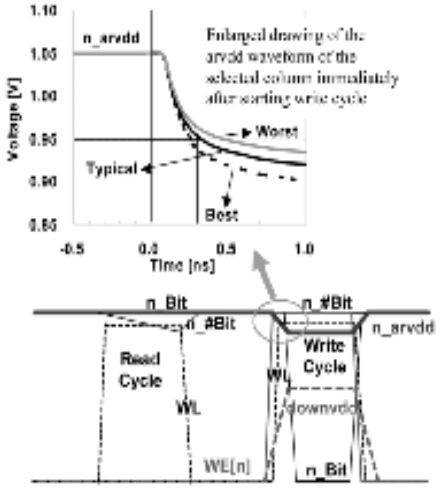


Fig. 13. The waveforms of read and write cycles using the read and write assist circuit.

Variation Components and specific impact on SRAM

Ref4 Miyamura2007

Motivation

- Explaining observed non-gaussian distribution in Vt sigma for min L design narrow devices in 65nm and beyond

Claims

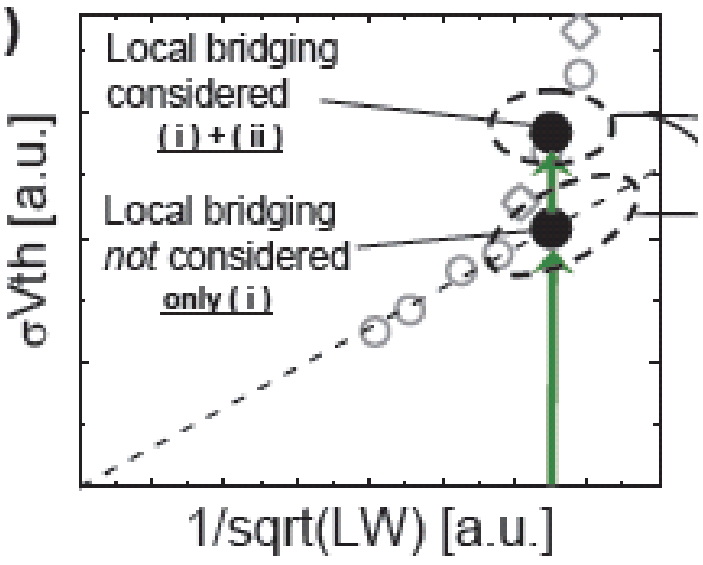
- 3-D simulations show origin of observed non-gaussian Vth dist
- Deviation from Pelgrom relationship observed for min L devices in 45nm
- Appropriate cell design overcomes issue

Method

Modeled discrete doping distributions using Monte Carlo implantation, thermal diffusion, line edge roughness or line width roughness (LWR). They simulated the details of the implantation angles doses and annealing conditions. Generated multiple devices and constructed a compact model to reflect these simulated devices.

Local bridging (LB) for min L devices resulting in non Gaussian asymmetric vt distributions.
Longer than min L and higher channel doping needed for SRAM devices beyond 65nm.

Major results



The Pelgrom plot showing the deviation they observe in hardware and in simulated distribution when the LB effect is included.

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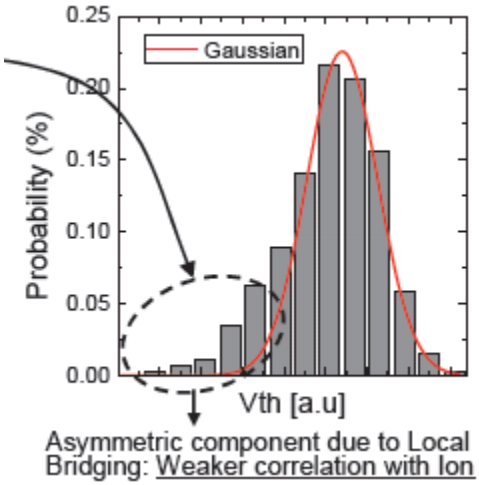

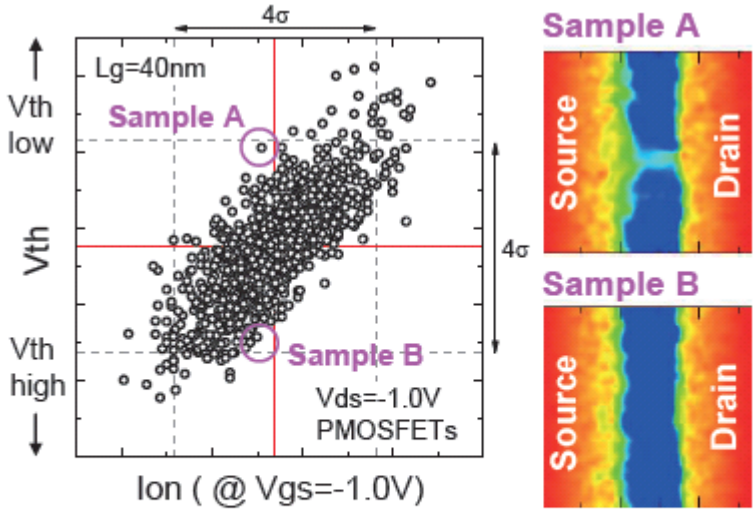

Fig.6: Typical examples of large-Vth-deviation with almost identical I_{ON}. , i.e. Samples A and B. The sample A has an accidental local-connection for the carrier(hole) distribution obtained from atomistic 3D-TCAD simulation.

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Major Results – explaining / reproducing observed hardware behavior with simulation results

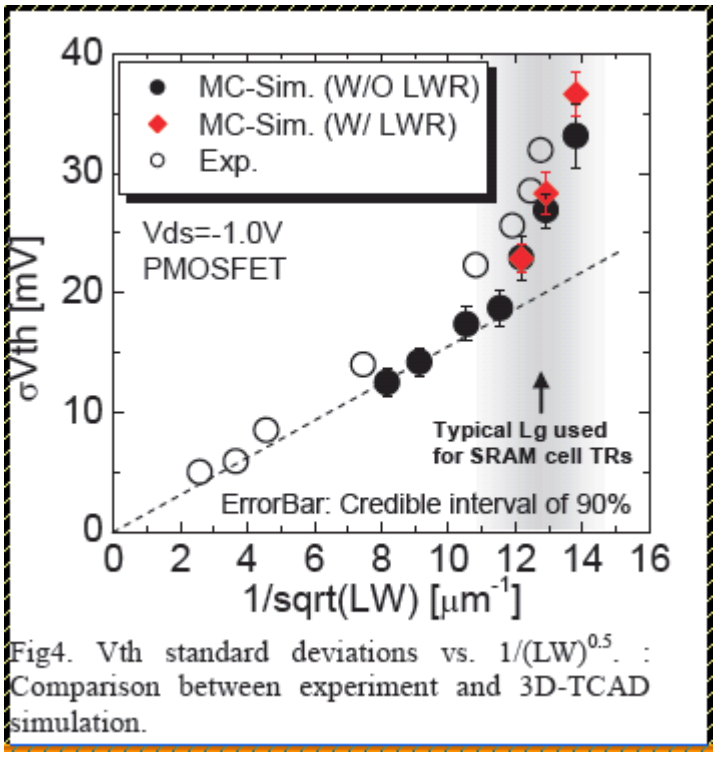

Fig4. Vth standard deviations vs. $1/(LW)^{0.5}$. : Comparison between experiment and 3D-TCAD simulation.

Ref3 Grossar2006]

Motivation

- How to define method of optimizing SRAM cell given design requirements

Claims

- A method to minimize the leakage power of a SRAM cell while satisfying conflicting functionality and delay constraints, under the technology variations

Method used

Authors use a statistical approach to compare access stability, write trip point, access time, leakage power and area.

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Major Results

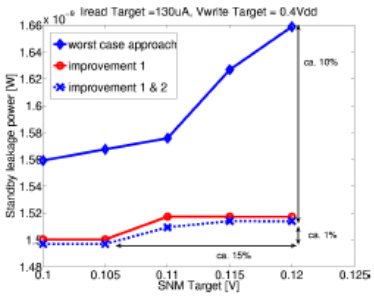

Figure 4. The optimized standby leakage power of the cell is shown versus SNM targets.

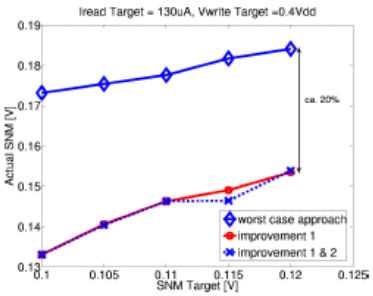

Figure 5. The actual SNM of the cell is shown versus SNM targets.

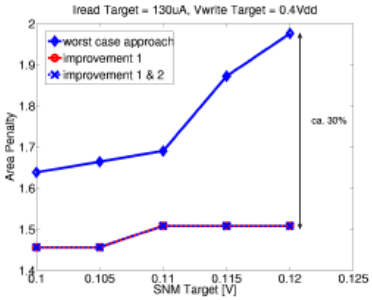

Figure 6. The area penalty of the cell is shown versus SNM targets.

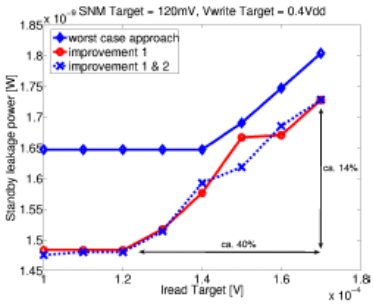

Figure 7. The optimized standby leakage power of the cell is shown versus Iread

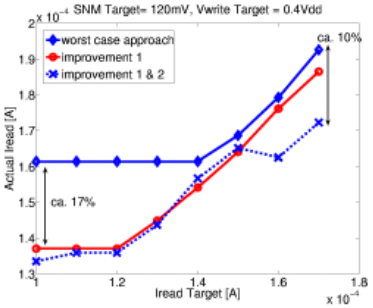

Figure 8. The actual Iread of the cell is shown versus Iread targets.

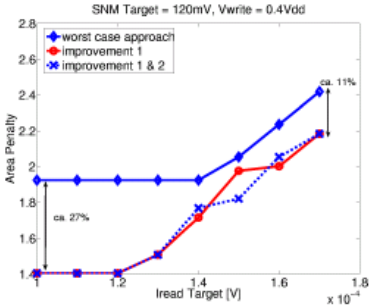

Figure 9. The area penalty of the cell is shown versus Iread targets.